Magnetic Resilience in Motion: Evaluating STT-MRAM Chips for Automotive Applications

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A replacement memory technology -- magnetic random-access memory (MRAM) -- has been introduced and is today under adoption by car chipmakers as it answers system requirements for more advanced vehicles.

THE AUTOMOTIVE INDUSTRY IS USING memory chips in vehicles for engine control units, such as on-board instruments and sensors, cameras, advanced driver assistance system (ADAS), and mapping systems; a count of 20 to more than 100 MCUs (Micro-controller Units) can be found in all cars fabricated today from entry-level to luxury ones [1].

After about 40 years of wide scale deployment of electrical charged based memories such as embedded flash (eFlash) and Static Random Access Memory (SRAM), a revolution in embedded memory technology is happening. Indeed, MRAM, based on the electronic spin-transfer torque effect (STT), is now entering into wide scale deployment as embedded memory in MCU applications. STT-MRAM presents stellar performances by very well compromising speed, power consumption, endurance, and scalability. It has already been introduced at 22nm technological node to replace eFlash memory in CMOS and FD-SOI processes for consumer wearable and IoT products [2,3]. It has also been presented on a 16nm FinFET process by TSMC [4] and 14nm by Samsung [5]. Recently, TSMC confirmed STT-MRAM commercial deployment on 16nm FinFET in a partnership with NXP [6].

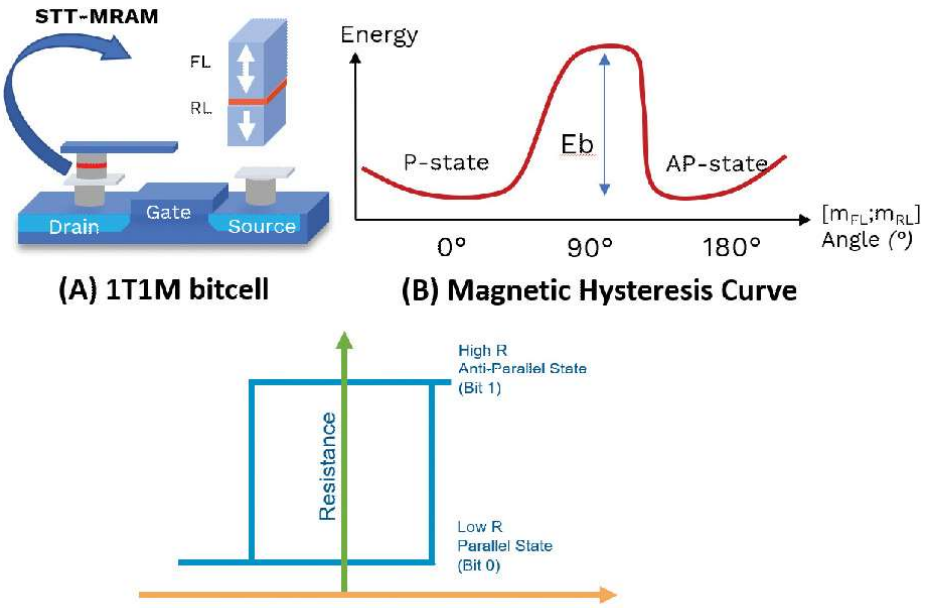

Figure 1. STT-MRAM description.

According to Objective Analysis and Coughlin Associates, in a report "*Emerging Memories Enter the Next Phase*," emerging memories have started a growth surge and should climb to become about a $44 billion market by 2032.

MRAM is by nature a magnetic memory, sensitive to certain types of magnetic fields and the adoption in automotive applications is on-going today. However, because magnetic fields can surround the STT-MRAM chip in vehicles, the chip's resilience under exposure to an external magnetic field became a critical part of the MCU test and qualification processes. Indeed, there are many different sources of magnetic fields in cars, such as magnetized wheels, alternators, electrical motors of windows lifters, and starters.

Permanent magnets are also integrated in systems for seat belt detection, door positioning, ABS and more.

The magnetic nature of STT-MRAM

STT-MRAM is a resistive memory, and the information (bit 0 or 1) is stored by the resistance value of the device. The memory bit-cell is composed of the Magnetic Tunnel Junction (MTJ) connected to a transistor or a switch selector used to route current in the MTJ for reading and writing. The MTJ is placed in the backend of line of a logic manufacturing process and positioned between two metallization layers (FIGURE 1a).

The MTJ is constructed by a stack of thin films including two magnetic ones separated by a thin enough insulator barrier to enable current tunnel effect. Each of these two magnetic layers has an intrinsic magnetization oriented in the up or down direction perpendicular to the wafer. If the two magnetic orientations are in the same direction, the MTJ resistance is in parallel state and has a low resistance value (bit '0') and if they are in opposite direction, it is in anti-parallel state and has a high resistance (bit '1'). The switching from one state to another can be triggered by temperature, current or magnetic field as long as the quantity of energy provided by the stimuli overcomes the energy barrier Eb (Fig. 1b). In the stack of thin films, a set of magnetic layers are used to give a reference orientation (called reference layer) and another layer is used to switch when writing the memory (called free layer). The free layer requires less energy to switch and can be seen as the active magnetic layer during memory operation. In the end-product operation, the writing of the MRAM by controlled switching of the free layer is made by passing an electronic current through the MTJ. At a certain threshold, the current switches the free layer by spin transfer torque.

STT-MRAM, from its magnetic nature, is sensitive to an external magnetic field. For example, to control the magnetic properties of STT-MRAM during the manufacturing process, the MRAM cells are tested under application of external magnetic field perpendicular to the MTJ surface. The magnetic hysteresis curve of the MTJ (Fig. 1c) is measured to evaluate the properties of the MTJ such as the ratio of the resistances in low and high states, the ability of changing the free layer states, the stability of pin layer…Even though in the application, STT-MRAM is operating only by use of electrical current, the level of magnetic strength to switch the free layer is normally a specified parameter to control the STT-MRAM. Depending on the stack and properties chosen for the MTJ and based on diameter in the range of 50-100nm, the free layer switching field are targeted in the range of 200 to 400mT and pin layer switching field in the range of 800mT to 1.6T, all with a direction oriented perpendicular to the MTJ surface.

Magnetic field in a vehicle

STT-MRAM deployment into automotive products requires quantifying the level of magnetic immunity of the memory as well as the level of magnetic field that are possibly present in the context of the end application.

From the literature, stray and propagating magnetic field are generally found to be lower than 5µT in the frequency range of 5 to 2kHz [7, 8]. As comparison, the Earth magnetic field is in the range of 25 - 65µT, depending on geographical position. The highest source of magnetic field in a car could originate from permanent magnets presenting a static field. Thus, we empirically evaluate the magnetic stray field over a bandwidth of DC-500Hz in different types of cars (Renault Clio, BMW i3, Peugeot 308). The magnetic field is measured at motor, alternator, doors, battery, fusebox, speakers and breakers areas and were recorded using calibrated I3C 3D Hall probe from Senis AG [9]. The levels of magnetic field measured in each considered case are illustrated in **FIGURE 2** and are shown in the range of less than 1mT at distances of more than 1 cm. The exact magnetic source position being in some cases unknown. The last right point of the graph illustrates the commonly used Neodymium permanent magnet of car phone holder. It presents here a magnetic field of 250mT at its surface and such magnets can present magnetic field in the range of amplitude for example of 100 to 500mT at the magnet surface. The field strength decreases quickly with the distance R as it is proportional to $1/R^3$[10]. As an example, for a cylindrical permanent magnet of 500mT, the magnetic field at

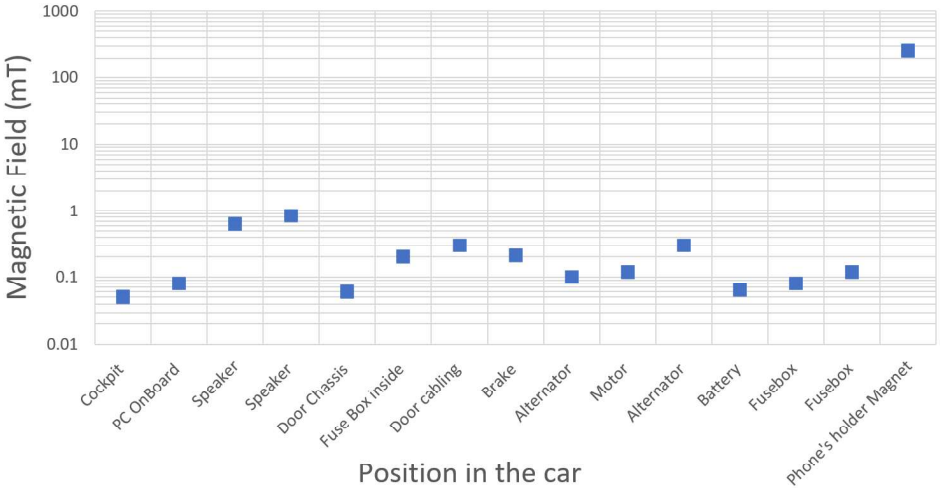

Figure 2. Stray fields in a car measured at different positions .

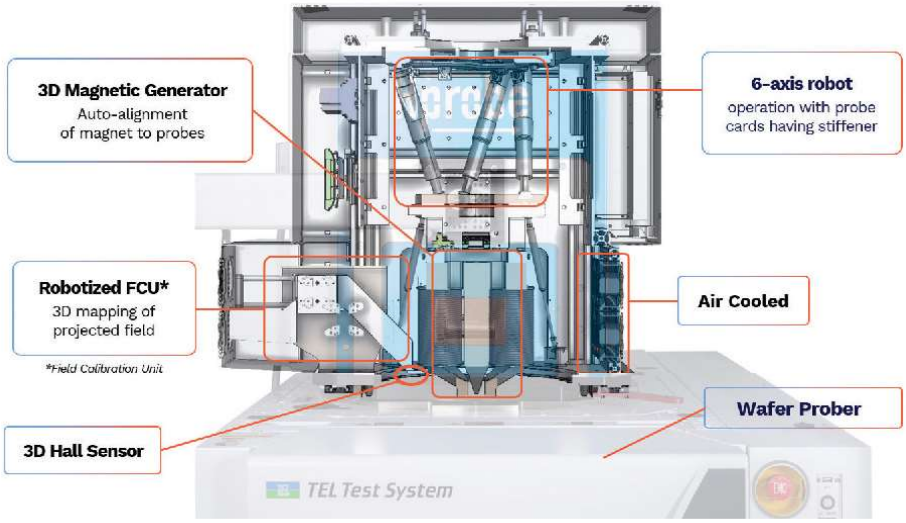

Figure 3. Magnetic test head cross for magnetic immunity tests, cross.

5mm distance is in the range of ~40mT and of 7mT at 1cm distance [11].

STT-MRAM magnetic immunity

In STT-MRAM, the probability of switching the free layer at a certain field increases with the time the MTJ is exposed. This probability is characterized by MRAM manufacturers from Bit Error Rate (BER) measurements under external field exposition. BER defines the ratio of switching error count over the total number writing/reading events requested. BER targeted levels are of less than one switching error per millions of events. The BER dependance to external stimuli like temperature and magnetic field stimuli have been studied and published by MRAM foundries (TSMC [12]], Samsung [13]], GlobalFoundries [14]). Positive temperature and external magnetic field at certain fields and angle produce an equivalent reduction of the energy barrier between the two states resulting in an increase in the BER.

The worst case being where field, and temperature are applied simultaneously. STT-MRAM manufacturers provided magnetic immunity specification of the memory as well as guidelines to specify magnetic immunity and shield the MRAM if this is required by the application [15,16]. Depending on test conditions, published data [11-15,17] report magnetic immunity levels at BER less than ≤ 1ppm with 100mT static field exposed during more than an hour at ambient temperature and in the range of 25 to 50mT at high temperature. The dependance of the BER to the field angle of the external field vector at an angle of 45° between the plane of the MRAM chip is expected to be the worst cases [12,15].

During the MRAM manufacturing process, magnetic immunity is evaluated. The wafers are heated for a specified time and exposed simultaneously to a vectorial magnetic field of controlled strength and angle. During and after this exposition, the Bit Error Rate is verified depending on the test mode: stand-by and active [14]. Stand-by immunity tests consists of applying an external field to the memory chip without executing any writing and reading operation. Active mode consists in reading or writing while applying the external field to the memory [14].

Testing STT-MRAM Magnetic Immunity

To verify magnetic immunity, Hprobe has designed a magnetic ATE using a unique magnetic generator that enables STT-MRAM magnetic immunity tests at wafer level. To cover all different possible sources of magnetic field present in the end applications, which is particularly important for Automotive chips, we designed a 3D magnetic field generator capable of applying a vectorial field with the XYZ components of direction controlled. The magnetic generator is integrated into a test head docked on the top plate of a wafer prober, as illustrated in **FIGURE 3**. The vectorial field is directly projected at wafer level to enable the evaluation of magnetic immunity before the packaging and assembly process. The test head integrates a hexapod robot used to align the generator with the electrical probe needles and the wafer under test. To calibrate and monitor the projected field on wafer, the system integrates a Field Calibration Unit (FCU) composed of a two-axis robot carrying a 3D hall sensor. The FCU can map the magnetic field in a spatial volume around the position of the test, with a grid resolution of less than 10µm. The test head is air-cooled and embeds a set of temperature sensors, controllers, and safety interlocks. The magnetic instrument is driven by an electrical rack and proprietary software interfacing with the electrical memory tester. The memory tester provides the electrical stimuli and sensing for BER tests and operates synchronously with the magnetic field projection on the wafer. The instrument is designed to reach the required level of magnetic field strength and angles to cover all types of application requirements including Automotive. The maximum out-of-plane perpendicular field is 700mT to voluntary switch the free layer, and maximum in-plane field of 200mT. The projected area on the wafer is in the range of ~3x3mm² to ~50x50mm² depending on the hardware configuration and magnetic field requirements. The projected area is sized to illuminate one or multiple STT-MRAM memory arrays depending on the magnetic immunity test case. The vectorial 3D magnetic generator is operating as a 3D magnetic arbitrary waveform generator for both static and dynamic fields projection simulating the chip exposition in the Continued on page 53

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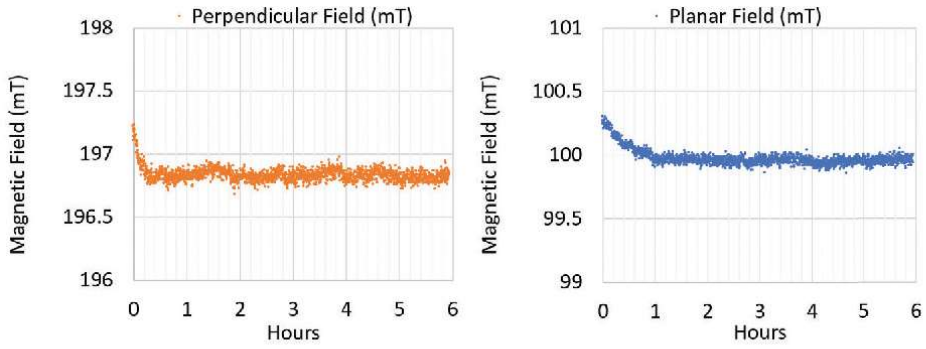

Figure 4. Illustration of static field stability while applied continuously for 6 hrs.

end-application. **FIGURE 4** illustrates the application of static out of plane and static in-plane field component at 200mT. The field is shown here to be applied continuously for 6 hours. After the first stabilization period, field variation within 0.1mT is shown. Stress with vectorial field at controlled and variable angle can be also executed like on a rotating field pattern illustrated in **FIGURE 5**. Dynamic out of plane rotating field with constant norm of amplitude at above 100mT is plotted to simulate a vector field coming from any direction in a plane that is perpendicular to the chip surface. The system can expose the MTJ by controlling the field strength, angle of vector and duration of exposition simultaneously with BER tests.

Summary

STT-MRAM technology is revolutionizing traditional charged based memory and its large deployment is now initiated. The driving applications for its deployments are today wearable, IoT and automotive. We illustrated empirically that in a car, the parasitic magnetic fields measured are very low compared to the switching field of the free layer. If the source of field is a permanent magnet, then the distance to the magnet must be at a controlled distance as the magnetic field decrease very quickly with it. MRAM manufacturers specify the magnetic immunity at a bit error rate of less than 1ppm at magnetic fields amplitude levels which are 20 to 100 times larger than all the measurements performed here. Nevertheless, for automotive applications, it is mandatory for safety of the system that data are safely stored and available in the memory [18]. To control STT-MRAM magnetic immunity during the manufacturing process, the wafers are stressed by a vectorial magnetic field of controlled strength and direction to evaluate the Bit Error Rate.

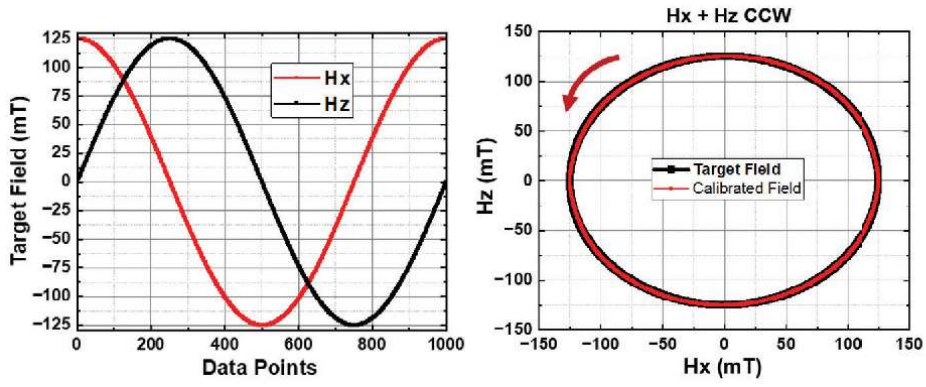

Figure 5. Illustration of rotating field in the XY direction for angular resolved immunity tests.

The level of resilience to a certain level of magnetic field and specific angles are then to be compared with the context of end application. If the MRAM chip has immunity specifications at below the level of magnetic field present in the end application, several solutions are already available such as the use of magnetic shielding in the chip packaging. System level consideration also enables several possibilities like guarding, by design, a distance to avoid any presence of permanent magnet. These solutions being on top of already implemented Error Correction Code (ECC) algorithms used to correct unwanted switching events within the memory. SD

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